FIELD EMITTER ARRAY RF AMPLIFIER DEVELOPMENT PROJECT

ARPA CONTRACT #MDA 972-91-C-0028

PHASE ONE, OPTION 1

QUARTERLY R&D STATUS/TECHNICAL REPORT #7

4/16/93 - 7/15/93

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Title of Work: Field Emitter Array RF Amplifier Development Project
ARPA Contract #MDA 972-91-C-0028
Phase One, Option 1

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MCNC Field Emitter Array RF Amplifier Development Project
Phase One, Option 1: Cathode Technology Development
ARPA Contract MDA 972-91-C-0028

Seventh Quarter – July 1993

Key Ideas

Develop field emitter arrays with a cutoff frequency above 1 GHz, total current greater than 5 mA, and 5 A/cm^2 current density with the gate electrode potential less than 250V. Demonstrate these characteristics for greater than 1 hour lifetime.

Reduce capacitance and increase transconductance of field emitter arays to improve frequency response. Focus on development of tall emitter columns to minimize capacitance. Evaluate low work function materials and metals as emitter surface coatings, reduce gate dimensions, and improve tip sharpening to increase transconductance. Fabricate large arrays with dense tip spacing to increase total current.

Examine various test methods to permit characterization of more devices per test cycle.

Major Accomplishments:

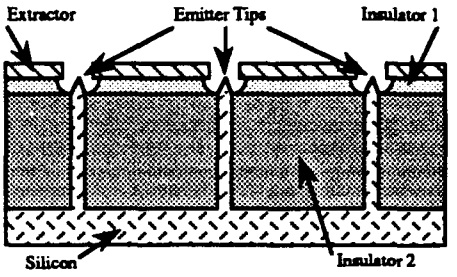
New mask set with larger arrays and increased tip packing density has been designed and fabricated. First fabrication run of 2 μm column devices with the new mask set complete, second run is proceeding on schedule. Lot origination for two runs of 4 μm column devices is complete.

DC test data from the first run shows yield on a 3,255 tip array, producing > 1 mA of current at > 1 A/cm^2 current density for > 1 hour with the gate electrode potential less than 250V. A 1,197 tip array delivered > 1 μA per tip under the same test conditions. Equipment for whole-wafer testing has been received and is being installed.

A process control statistical analysis has been conducted and implemented to improve tip uniformity and yield on large arrays. The overall process flow has been frozen, allowing changes and improvements only at the individual step level.

Low work function and metal coating studies have started. Materials under study are in-house or have been ordered.

MCNC Silicon Field Emitter with Column



Major Milestones – This and upcoming quarter:

Deliver sample devices for testing and SEM inspection data from first device fabrication run. Characterize DC performance of devices from this run. Complete second fabrication run.

Install and debug the whole-wafer test system. Continue the DC characterization and reliability testing program for Option 1 devices. Install and debug the equipment needed for the in-house RF testing program. Screen completed devices and prepare selected devices for RF testing at Litton subprogram site.

Complete the second fabrication run of 2 μm column devices. Complete the third and fourth device fabrication runs; two runs of 4 μm column devices. Begin the lot origination process for last two runs of 4 or 6 μm column devices. Incorporate low work function and metal coating into fabrication process flow.

Field Emitter Array RF Amplifier Development Project
Phase 1, Option 1

I. Executive Summary

- ARPA exercised the option to continue funding to the MCNC field emitter program for an additional year under Option 1 of the original contract. Final contract approval was obtained on April 16, 1993.

- Devices from the first fabrication run of 2 μm column emitters were tested. Anode currents in the 100 μA – 1 mA range were observed at actual gate potentials of less than 250 V in several cases. Two 3,255 tip arrays yielded currents greater than 1 mA, corresponding to current density greater than 1 A/cm^2. The second device operated under these test conditions for over an hour. Another device with the same overall area, but only 1,197 tips, produced a total current corresponding to an average of greater than 1 μA per tip.

- Devices from previous fabrication runs were also tested. These devices produced per tip currents from 640 nA to 2.1 μA. Testing of field emitter devices at ambient pressure was proposed as a more time-efficient and economical method than testing under vacuum, and initial experiments were carried out. Pre-test cleaning of the devices was also investigated.

- A process integration analysis was performed to optimize the process in an effort to increase yield on large arrays. Using the results of this analysis, yield was achieved on arrays over 15 times larger than the largest previous good arrays. This yield was also a result of improved uniformity in the photolithography.

- Modifications to the oxidation sharpening process produced sharp tips with much shorter processing times. A second oxidation sharpening step was developed to insure uniformly sharp tips with average radius less than 200 Å.

- The gate and backside metal systems were changed to improved adhesion and wire bond reliability. Metal solders can now be used for die attach, eliminating the need for organic conductive epoxies with poor vacuum compatibility.

- The vacuum testing and microencapsulation bonding system was modified in response to postponement of the wafer bonding experiments requested by ARPA. The bonding chamber was converted to an additional testing chamber to improve test throughput. Equipment for whole-wafer testing in the test chamber has been acquired and is being installed.

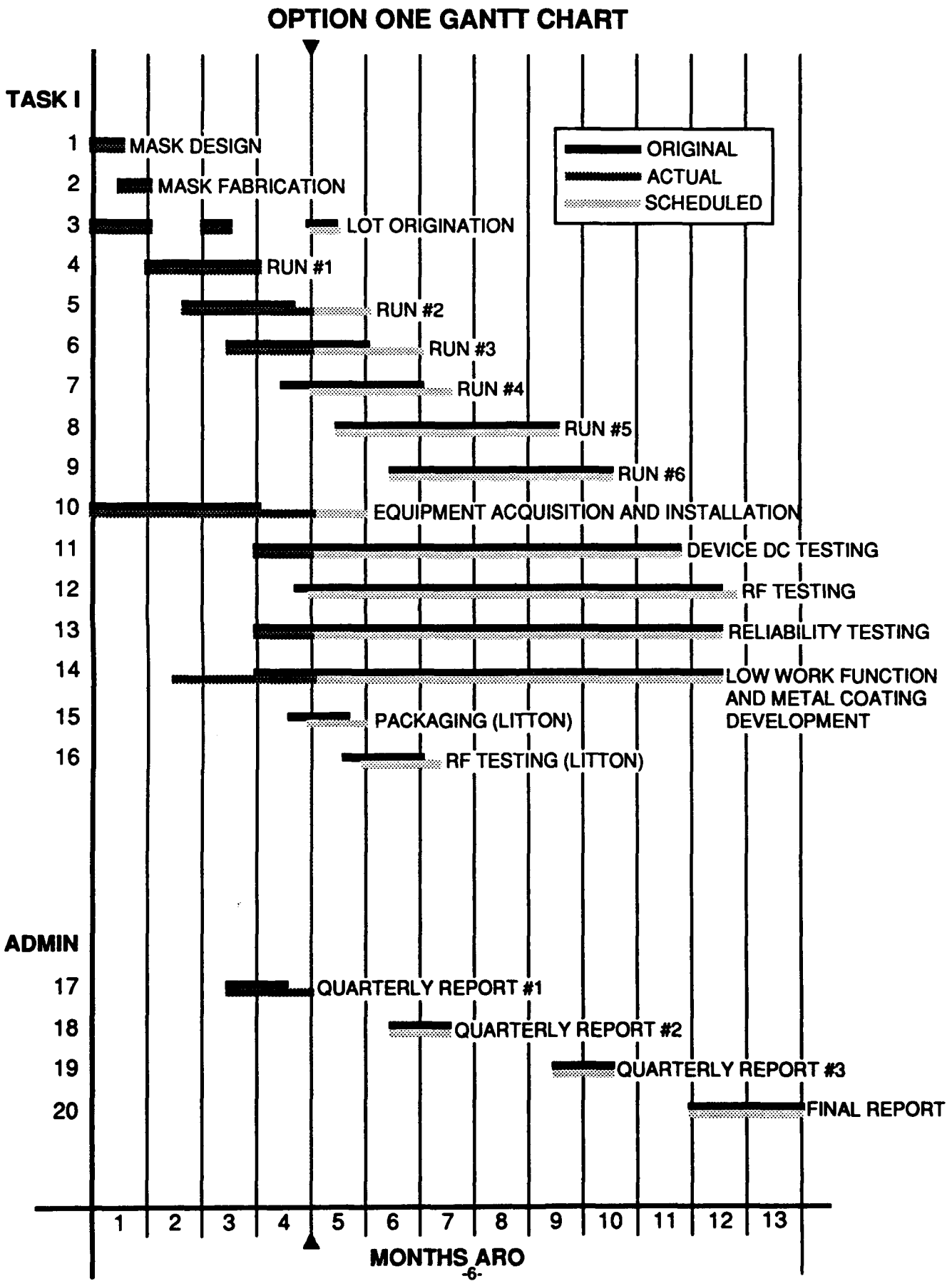
- A new reticle set was designed and fabricated for the Option 1 device fabrication runs. The reticle set incorporated increased array size and tip packing density, but also provides devices for low work function and metal coating development and per-tip current studies.

- Possible low work function and metal coating materials have been identified. Some of the materials have been obtained and characterized. A deposition process for thin films of TaN is being developed in-house.

II. Milestone Status:

Task	Completion Date	
Milestones	Original	**Complete** Expected
Complete design and fabrication of new reticle set. Complete lot origination process for two runs of 2 μm column emitter arrays. (MCNC)	5/93	**5/93**
Complete first run of field emitter arrays (2 μm column). Complete lot origination process for two runs of 4 μm column field emitter arrays. (MCNC)	7/93	**8/93**
Complete acquisition and installation of whole wafer DC test and RF measurement equipment. Begin in-house device DC characteristics and reliability testing program. (MCNC and Duke)	7/93	8/93
Begin low work function and metal coating development. (MCNC)	7/93	**6/93**
Complete second run of field emitter arrays (2 μm column). Deliver devices to Litton subprogram for packaging and RF testing. (MCNC)	9/93	9/93
Begin in-house device RF testing program. (MCNC)	8/93	8/93
Complete third run of field emitter arrays (4 μm column). Complete lot origination process for two runs of 4 or 6 μm column field emitter arrays. (MCNC)	10/93	10/93
Complete packaging, begin RF testing of field emitter amplifier modules. (Litton)	9/93	9/93
Complete fourth run of field emitter arrays (4 μm column). (MCNC)	10/93	11/93
Complete RF testing of field emitter amplifier modules. (Litton)	10/93	11/93
Complete fifth run of field emitter arrays (4 or 6 μm column). (MCNC)	1/94	1/94
Complete sixth run of field emitter arrays (4 or 6 μm column). (MCNC)	2/94	2/94
Complete all contract activities. Deliver devices, data, and other related material to ARPA. Complete and deliver final report according to contract stipulations. (MCNC)	4/94	4/94

Task	Completion Date	
Deliverables	Original	**Complete** Expected
Plots of new mask design set available for inspection by ARPA personnel if desired.	5/93	**5/93**
Sample devices from the first run of field emitter arrays (2 μm column) with SEM inspection data.	7/93	8/93
First quarterly R&D status/technical report.	8/93	**8/93**
Sample devices from the second run of field emitter arrays (2 μm column) with SEM inspection data. Performance data from first run.	8/93	8/93
Sample devices from the third run of field emitter arrays (4 μm column) with SEM inspection data. Performance data from second run.	9/93	10/93
Sample devices from the fourth run of field emitter arrays (4 μm column) with SEM inspection data. Performance data from third run.	10/93	11/93
RF amplifier module performance data from Litton subcontract.	10/93	11/93
Second quarterly R&D status/technical report.	11/93	11/93
Sample devices from the fifth run of field emitter arrays (4 or 6 μm column) with SEM inspection data. Performance data from fourth run.	1/94	1/94
Sample devices from the sixth run of field emitter arrays (4 or 6 μm column) with SEM inspection data. Performance data from fifth run.	2/94	2/94
Third quarterly R&D status/technical report.	2/94	2/94
Low work function and metal coating development results. Performance data from sixth run. Reliability test data for all devices. Final Technical Report – Option 1.	4/94	4/94


OPTION ONE GANTT CHART
TASK I
1 MASK DESIGN
2 MASK FABRICATION
3 LOT ORIGINATION
4 RUN #1
5 RUN #2
6 RUN #3
7 RUN #4
8 RUN #5
9 RUN #6
10 EQUIPMENT ACQUISITION AND INSTALLATION
11 DEVICE DC TESTING
12 RF TESTING
13 RELIABILITY TESTING
14 LOW WORK FUNCTION AND METAL COATING DEVELOPMENT
15 PACKAGING (LITTON)
16 RF TESTING (LITTON)
ADMIN
17 QUARTERLY REPORT #1
18 QUARTERLY REPORT #2
19 QUARTERLY REPORT #3
20 FINAL REPORT
ORIGINAL
ACTUAL
SCHEDULED
1 2 3 4 5 6 7 8 9 10 11 12 13
MONTHS ARO

III. Technical Progress:

1.0 Electrical testing and high-frequency performance measurements.

1.1 Devices from the first fabrication run of 2 μm column emitters were tested. Several arrays produces current in the 100 μA – 1 mA range with actual gate potential less than 250 V. Two 3,255 tip arrays yielded currents greater than 1 mA, corresponding to a current density greater than 1 A/cm^2. Plots of the raw I-V curve data for these two arrays are shown in Figures 1 and 2. With the gate potential corrected for the effects of the series resistor in the gate lead, the data is re-plotted in I-V curve, Fowler-Nordheim, and Frenkel-Poole format in Figures 3 and 4. The second device operated under these test conditions for over an hour, plotted in Figure 5.

Another device with the same overall area, but only 1,197 tips, produced a total current corresponding to an average of greater than 1 μA per tip. The raw data for this device is shown in Figure 6, and the curves with the corrected gate voltage are shown in Figure 7. The unusual noise in the data from this device may be a result of instabilities in the anode voltage. This is under further investigation.

RF testing will begin in the next quarter.

1.2 Devices from previous fabrication runs have been tested, showing average per-tip emission current of 640 nA for a 100 tip array at a corrected gate potential of 150 V. Single tips have shown up to 2.1 μA at a gate potential of 80 V (corrected). With the anode potential at 2 kV, the gate current is usually less than 1 percent of the total emission current. When a device was emitting, even if the gate bias is held constant, the gate current remains constant for some time, then suddenly surges into the tens of μA range just before the device fails. SEM photos taken after the tests reveal melted gate metal around some of the tips, ranging from just a few tips up to about 80% for 100 or 200 tip arrays.

1.3 It was proposed that field emitter arrays could be tested in an inert ambient at normal pressure as a more efficient and economical method than testing under vacuum. If testing at ambient is possible, rapid screening of a large number of devices for gate metal shorts would be possible. The idea is based on the shape of the Paschen curve for plasma discharge formation versus ambient pressure. The fact that the distance between the gate and the tip is so small further reduces the possibility of plasma discharge at normal pressure. Initial experiments suggest, however, that the formation of a plasma is possible under these conditions. If a plasma is induced during testing, it will damage the device under the test. It may be too early to conclude that the testing under inert ambient is not feasible, but apparently more experiments are required to reduce the concept to practice. The initial experiments were conducted on devices with relatively large gate hole openings (3.0 – 3.5 μm). The work will continue, using devices with much smaller gate hole openings (1 μm range).

1.4 Cleaning the field emitter arrays immediately prior to testing appears to play an important role by removing any residual oxide left on the tips after processing. Some devices were cleaned using reactive ion etching. Their performance was somewhat better than devices tested with no cleaning. In addition, equipment that will allow *in-situ* hydrogen plasma cleaning of the devices is being installed in the test chamber. The hydrogen plasma will reduce the native oxide layer that forms on the surface of

the silicon tips, as well as converting any residual hydrocarbons to volatile species that can then be pumped away with the other residual gases.

2.0 Device processing.

2.1 A general review of the entire field emitter fabrication process was held for the purposes of formalizing the process and identifying possible new problems. In order to gain fresh insights on the process as a whole, several MCNC engineers external to the field emitter program were invited to the meeting. During these discussions, it was suggested that the fabrication process should be further analyzed on a step-by-step basis using a methodology known as process integration analysis (PIA). PIA is an engineering technique in which known variations in each process step are taken into consideration at every level so that steps that introduce the greatest variations can be identified and better controlled. It also allows a range of possible values for each geometric parameter of the final structure to be estimated.

The quantitative basis of PIA rests in the determination of target values for certain critical stages in the fabrication process flow. These target values incorporate the known variational data as parameters in the processing so that the final structure will satisfy the original specifications. An important assumption in calculating these values, however, is that extremes in the variation of each process step are unlikely to occur in direct succession at the same sites. That is, the variations in each process step are independent from one another. Thus, an accumulation of worst-case effects on any particular device can be dismissed as highly improbable, and need not be considered a determining factor for process parameters. A more conservative variant of this procedure that can also prove helpful is to use the variational data to estimate minimum and maximum values of each geometric parameter after each step. Either way, by examining the individual process variations, a statistical distribution of the resulting geometries can be predicted.

This analysis was applied to the first fabrication run of 2 μm column devices with the new mask set for Option 1. Recent records of each processing step were first reviewed to determine reasonable variational data, and then an calculation was made to determine how the variations would affect whatever processing steps followed. At the conclusion of each step, a range of values for each geometric parameter was generated based on the minimum and maximum values that were possible in worst case conditions. For comparison purposes, the PIA target values were also calculated for each step in the process flow.

Once the key relationships between process parameters and known variations had been established through this type of analysis, they were then entered into a spreadsheet program to allow convenient modification. With this capability, the min - max ranges for the field emitter structural dimensions are quickly recalculated every time the input parameters and/or variational data is changed. Actual data from the post-RIE nitride etch step of the first run was inserted into the spreadsheet program to generate accurate values for the structural dimensions that were likely to result. These numbers were then used in a finite element analysis of the induced electromagnetic fields to predict the most probable electrical characteristics of the finished structure.

2.2 In the photolithography that defines the pattern that forms the basis for etching the emitter tips, the primary goal is uniformity in the dots of photoresist that form the mask for the nitride etch. The uniformity at this point in the process is particularly important, as any non-uniformities generated at this step will propagate through the process flow and contribute to non-uniformity in other geometric parameters such as gate hole diameter and total emitter height.

Uniformity is judged by a collection of critical dimension (CD) measurements of dots, and a subjective judgment on the circularity of the dots. A dot should be circular, but it may be elliptical or otherwise distorted due to lack of optimum focus and lens aberrations. Sometimes a distorted dot will give a good CD, so both criteria must be used to get a reliable measure of uniformity. If dots are reasonably round, the variation in CD is a good measure of non-uniformity.

Our patterning of the first lot was done using the light field reticle of the new reticle set on the new I-line stepper at MCNC, a superior tool to the H-line steppers that were used in the previous device runs. Results from the first run yielded uniformity with a 3-sigma variation of 0.1 μm, as good as the best uniformity achieved on the H-line steppers. The variation is measured over 25 different wafers, at 25 locations on each wafer to insure valid statistical samples. The observed circularity of the dots was excellent, with minimal distortion.

The new reticle set includes a dark field copy of the emitter mask level. Experience indicates that there is an inherent uniformity advantage to the dark field process, despite some added complexity. We are currently developing a process on the I-line for this reticle, and may use it on the third lot in the project. This will also depend on the results of the process integration analysis incorporating this process, that should indicate whether improving the 3-sigma variation by 10 or 20 nm is worth the added complexity of the dark field process.

2.3 Several experiments were performed to identify the best method of oxidation sharpening of the silicon tips. The experiments tested a change in the original process of dry oxidation sharpening to the more efficient wet/dry/wet oxidation technique. The primary advantage of the wet/dry/wet process is increased rate of oxidation. The original dry oxidation sharpening method required up to 80 hours of processing time. With the new wet/dry/wet method the process time is reduced to several hours based on the amount of silicon to be oxidized. The proper oxidation time can be determined based on the tip width after anisotropic etch formation and the measured oxidation rate in the <100> plane of the silicon. The experiments were successful and sharp tips were formed.

The experiments further tested the effect of a second oxidation sharpening step as the last step on a completed device. These experiments were performed on sharpened tips from the first experiment that had not achieved the desired tip radius. The second oxidation sharpening creates a sharpened tip with radius less than 200 Å, based on SEM examination. This process was also successful, and is available for use on future runs if necessary.

2.4 Three metal systems were evaluated for use as the gate electrode and bonding pad material: a single 5000 Å layer of aluminum, a 500 Å layer of chrome with a 500 Å layer of tantalum and a 4000 Å layer of platinum, and a 500 Å layer of titanium

followed by a 4500 Å layer of platinum. A fourth system incorporating iridium is under consideration for future tests.

The aluminum gate and bonding pads adhered well to the gate insulator layer (silicon dioxide), but could not be wire bonded successfully. The difficulty was most likely due to the softness of the aluminum and the thinness of the metal layer. A noticeable adhesion problem was observed on the second system (Cr / Ta / Pt), especially in the bonding pad area where some curling and peeling of the gate metal was observed. The high stress of this film might be the main reason. The third system (Ti / Pt) was tested on one wafer. This system deposits uniformly, and passes the adhesion test (ASTM designation D3359-92a, "Standard Test Methods for Measuring Adhesion by Tape Test") for adhesion. This system also wire bonds well.

The backside metallization was changed from a single 5000 Å layer of aluminum to a 750 Å layer of titanium, 2000 Å of nickel, and 5000 Å of silver. This system will allow die attach with metallic solder rather than organic silver-loaded conductive epoxy, improving high-vacuum compatibility. Tin-silver solder with a melting point of about 221 °C will be used when bakeout of the vacuum test fixtures at temperatures up to 200 °C is desired. The metallization system is also compatible with lower melting point lead-tin solder when high-temperature operation is not required.

3.0 Vacuum testing and microencapsulation bonding system.

3.1 A qualification test of the vacuum bonding chamber heating coil was conducted for the primary purpose of running a pre-programmed heating cycle regulated by the system's Eurotherm temperature controller. Neither of the two previous tests had achieved and maintained a stable temperature for any length of time. With a practice pair of wafers loaded into the press (force set at 30 psi), the test program was set to stabilize at 600 °C for one hour. The heater control circuit failed and the coil temperature steadily rose to 774 °C, at which point it suddenly and sharply fell off, possibly indicating a loss of power to the coil. A post-test examination performed on the system revealed that the heating element (a replacement unit sent out to MCNC by Shrader Scientific) had broken in two symmetric places. In addition, both the coil and the underside of the quartz diffuser were covered with a grayish deposit.

The decision was made to discontinue all high-temperature wafer-bonding experiments in the bonding chamber, and to convert it to use as a secondary testing chamber. Even though the vacuum level would never be quite as high as achievable in the original testing chamber, the bonding chamber would theoretically have the capability of sample bake-out at up to 200 °C, instead of chamber wall bakeout. This modification could potentially double the testing capacity of the system for the ARPA field emitter project.

With this new direction in mind, repairs on the bonding chamber then focused on repair of the heater control circuit. The broken heating coil was removed from its quartz holder and was replaced by the original coil. Attempts at wiring the original coil into the new holder revealed, however, that a large resistance was present in parallel with the coil. This was the grayish metallic coating present over the surface of the holder, the result of some contamination process that occurred during the previous heating test.

It was decided that the most effective way of removing this material was to chemically clean the piece sequentially in HF/nitric and aqua regia. The quartz diffuser and ceramic spacer pieces were included in this cleaning. The cleaning produced excellent results, and the newly cleaned pieces were then successfully reassembled and wired into the bonding chamber. A brief test of the heating circuit immediately afterward demonstrated that the coil was receiving power (the temperature reached 400 °C), but the same lack of control by the Eurotherm programmer was evident.

Another attempt at running a temperature-controlled heating cycle with the Eurotherm was made with a 15 minute dwell time at 150 °C to simulate a sample bake-out process. Once again the heating circuit received power entirely unregulated by the controller, and the coil temperature peaked at 218 °C before the power was manually shut off. On a suspicion that the Eurotherm was improperly wired, the main power controller was opened up and examined the following day, revealing a shorted 40-amp solid-state relay. This relay was the principal means of regulating power flow to the heating coil. A new relay with a higher current rating was ordered and installed into the main power controller. A brief heating cycle taking the coil no higher than 200 °C was successfully performed, with the Eurotherm holding the temperature in line throughout the process.

3.2 Orders were placed for equipment intended for installation on the testing chamber as part of the whole-wafer testing system. This equipment included a 5.50 inch diameter viewport to allow placement of probes on the array electrodes, and a set of vacuum-compatible micro-manipulators. The viewport has been installed on the chamber. The micromanipulators are in-house and will be installed in the next quarter.

4.0 Other Developments.

4.1 The new reticle set for the ARPA Option 1 field emitter devices is completed. The die is a 1 cm x 1 cm square divided into nine sections. An overall view is shown in Figure 8. Each row of three sections has a different pattern, while each column of three has a specific emitter tip-to-emitter tip spacing ("tip pitch"). Each section of the top row contains four ("quad") arrays. The middle row sections contain arrays sized to meet customer requirements ("ARPA" and "Litton"), as well as arrays of CV dots for testing the gate oxide layer. The two rightmost sections of the bottom row contain one large array each. The leftmost ("experimental") section is further divided into quarters, with arrays for coating experiments and per-tip emission current studies.

Bonding pads are placed on the outside edges of the die sections where possible to facilitate wirebond attachment. A space of 8 mils (0.2 mm) is left between each section to allow for the dicing saw kerf. Each section forms a 3.2 mm square. Individual array dimensions are not particularly critical, except in the case of the customer specific arrays in the middle row.

The quad array section, shown in Figure 9, has four 1.3 mm square arrays evenly distributed within the section. The 1.3 mm square metalization area comprises a 1.3 x 0.2 mm bonding pad, a 20 μm metal border around the periphery, and an active area containing tips covering the remaining area. The number of tips in the active area will depend on the tip pitch.

The customer-specific array sections in the middle row have 9 arrays that are 0.001 cm square. This is the minimum size that can meet both the current density (5 A/cm^2) and total current (5 mA) requirements set forth in the ARPA contract. These are 0.4 x 0.5 mm rectangles with bonding pads oriented as shown in Figure 10. These arrays have an active area of 0.316 x 0.316 mm centered in one end of the rectangle. The remaining metalization acts as the bonding pad and border of the array. The three other arrays are 0.8 mm squares with a 4 x 8 mil (or about 100 x 200 μm) bonding pad in the center of one edge and a 20 μm border around the periphery. These arrays are the maximum device size that Litton can accommodate in their chip carriers, with the minimum size bonding pad required for ribbon bonding. Ribbon bonding should improve the RF performance of the arrays by minimizing series inductance in the leads. In the center of the section, a number is placed in the metalization mask to indicate the tip pitch in microns. This number is surrounded by an array of 100 μm diameter CV dots to be used for evaluating the quality of the gate oxide.

The bottom row contains two large arrays, one with 6 μm tip pitch and the other with 10 μm tip pitch. A 4 μm large array is not included, as fabrication of such a large array with such closely spaced tips was deemed unfeasible. The large array section, shown in Figure 11, contains a single 2.8 mm square array. The 2.8 mm square metalization area comprises a 2.8 x 0.2 mm bonding pad, a 20 μm metal border around the periphery, and an active area containing tips covering the remaining area. The number of tips in the active area again depends on the tip pitch.

The experimental section is further divided into quarters, with arrays for coating experiments and per-tip emission current studies. The quarters have a 0.2 mm street separating them, leaving each quarter 1.5 mm square.

The array for the low work function and metal coating experiments, shown in Figure 12, consists of 16 single tips distributed around a 10 mil (250 μm) circle in the center of the quarter. Each tip has a separate 0.1 x 0.2 mm bonding pad set in 0.1 mm from the edge, with the pad in the upper right hand corner 0.2 mm square to show die orientation. Each bonding pad is connected to one of the gate metal circles by a line 1 mil (40 μm) wide. The tip gate metal consists of the rounded end of the connecting line. With the spacing shown it will be possible to have all the tips under a single tungsten wire anode that can be placed very closely above the devices.

Figure 13 shows one of the quarters filled with square arrays for per-tip current studies. Arrays of 1, 2, 3, 4, 5, and 10 tips on a side are included. The tips in these arrays are arranged on a rectangular grid centered in the square of metal. The tip pitch is indicated by a number in the upper right-hand corner of the quarter. For consistency, the size of the square containing the array does not change as the tip pitch changes. The single-tip array is in a pad 50 μm square, the 2 x 2 in a 100 μm square pad, 3 x 3 in a 150 μm square pad, 4 x 4 in a 200 μm square pad, 5 x 5 in a 250 μm square pad, and 10 x 10 in a 0.5 mm square pad. A total of six 0.1 x 0.2 mm bonding pads are set in 0.1 mm from the edge of the quarter. Two across the top and bottom are set 0.5 mm apart, while two on the sides lie on the centerline of the quarter. The connecting metal from the bonding pad to the array pad will be 160 μm long, and centered on both pads.

The field emitter array structures can be fabricated with as few as five reticles. These are listed below.

1. A light-field mask with 1.6 μm diameter circular dots for the emitter tips in the active areas only.

2. A dark-field mask with 1.1 μm diameter circular dots for the emitter tips in the active areas only. The alignment verniers are in a different location from the ones on the light-field mask.

3. A light-field mask with chrome where the metalization will appear on the die. The CV dots appear on this mask.

4. A light-field protection mask with chrome covering only the active areas of the arrays, and the single tips in the array for coating studies. The edges should be approximately 10 μm in from the edges of the metalization mask.

5. An open field over the entire die (blank 1 cm square).

Although the I-line stepper is the photolithography instrument of choice in the fabrication of these devices, the reticles are compatible with any of the steppers at MCNC for greatest processing flexibility. The reticles use quartz glass for compatibility with the laser stepper, have DFAS alignment marks appropriate for the I-line stepper, with global alignment targets and I-bars compatible with the H-line stepper.

All of the arrays except those for the per-tip current studies of the bottom row use triangular rather than rectangular tip placement. This geometry increases tip packing density by about 15%, as shown in Figure 14. Three different tip pitches are used: 4, 6, and 10 μm. The different tip pitches produce different tip densities. The tip density in the horizontal direction is different from the density in the vertical direction due to the triangular packing. When the spacing between each of the tips is equal to t = 4 μm, the tip density in the vertical direction is 250 tips/mm and in the horizontal direction is 289 tips/mm. For t = 6 μm, the densities are 166 tips/mm (vertical) and 192 tips/mm (horizontal). For t = 10 μm, the densities are 100 and 115 tips/mm. Table 1 shows the approximate dimensions and exact number of tips per array for the various sections. The number of tips was determined by counting the dots in each array in the CAD program.

Table 1. Dimensions and approximate total number of tips per array.

Array	DARPA	Litton	quad	large
Tip Pitch				
4 μm	80 x 92 7,347	188 x 220 41,360	268 x 373 99,985	not used
6 μm	53 x 61 3,255	125 x 146 18,309	180 x 247 44,460	431 x 540 232,630
10 μm	32 x 37 1,197	76 x 88 6,648	108 x 149 16,092	263 x 319 83,850

From the 316 μm square arrays, the minimum current per tip required to meet ARPA total current specification can be calculated. For 10 μm pitch, 5 mA from 1,197 tips requires a current of 4.2 μA/tip. For 6 μm pitch, 5 mA from 3,255 tips requires a current

of 1.5 μA/tip. For the 4 μm pitch array with a total of 7,347 tips, 680 nA/tip is required. If the current density specification is met but not exceeded, the total expected current from each array is easy to calculate. Assuming that at 1 GHz, the modulated anode current is 10% of the DC anode current, and all of the modulated current is coupled into the 50 Ω output line, the RF power output from each array can be predicted as well. These predictions are shown in Table 2.

Table 2. Expected current and RF power from the arrays.

Array	ARPA	Litton	quad	large
DC Current	0.005 A	0.028 A	0.068 A	0.344 A
RF Power	12.5 μW	392 μW	2.31 mW	59.0 mW

To get 1 W of RF power under these assumptions requires a DC current of 1.41 A, or approximately four of the largest arrays. To get 1 W of RF power from the largest arrays on the mask would require a per tip current of 6.1 μA at 6 μm pitch or 16.8 μA at 10 μm pitch.

4.2 Coating of silicon field emitters with low work function materials is being investigated as an option in the MCNC's field emission device manufacturing process. Diode and triode structures with silicon emitters coated using a material with a lower than silicon work function should exhibit greater transconductances and smaller turn-on voltages, in comparison with uncoated devices. Additional requirements for suitable coatings include low (metallic or n-type semiconductor type) resistivity, high melting point, as well as mechanical and chemical stability at elevated temperatures and in an environment where ion bombardment can take place. The coatings also need to be amenable to the integration into silicon emitter process flows.

Low work function materials with required characteristics have been identified on the basis of a literature search. Some of the materials that potentially can be obtained in a thin film form using in-house capabilities, are given in Table 3, together with reported room temperature work function values, resistivities, melting points and potential deposition methods.

Table 3: Some Potential Materials for Silicon Emitter Coatings.

Material	ϕ (eV)	Melting Point (°C)	Resistivity (μΩ cm)	Deposition Method
TaN	1.85	3087	200	RF sputtering
LaB_6	2.7	2530	15	e-beam evaporation
ZrC	2.2	3530	170	e-beam evaporation
TiC	3.4	3257	70	e-beam evaporation
HfC	3.2	3890	40	e-beam evaporation
Cr_3Si	2.3	1770	40	e-beam co-evaporation of Cr and Si

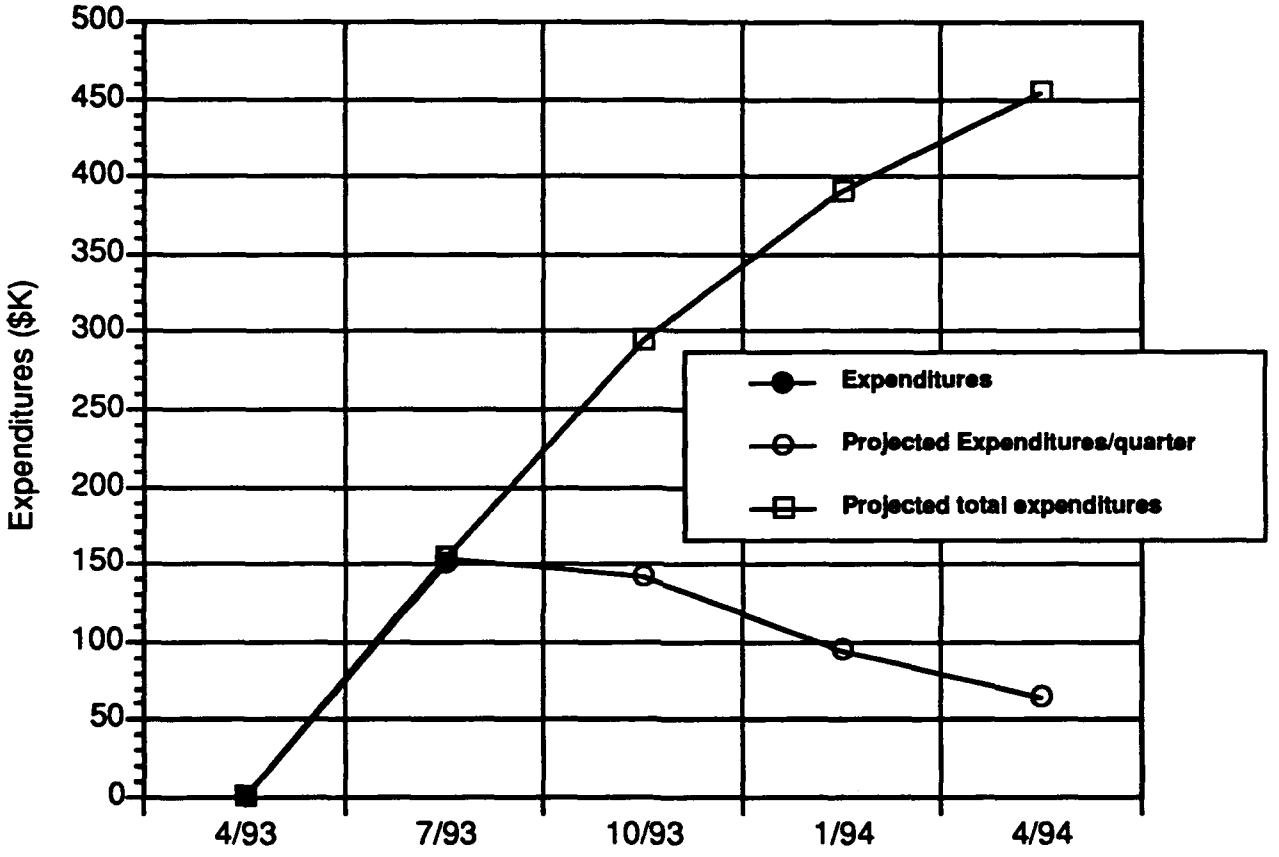
At the present time, we are engaged in the development of the deposition process for TaN. Thin films of TaN can be obtained in-house by means of a reactive sputtering of a pure tantalum target in a nitrogen atmosphere. First test runs have been performed

in a Perkin-Elmer 4450 RF sputtering system, using silicon wafers as substrates. After an initial optimization of the process conditions, such as the RF power level and partial pressures of nitrogen and argon, the sputtering produced mirror-smooth well-adherent films, with the growth rate of about 100 Å/min. The resistivity of films ranged from 210 to 220 $\mu\Omega$ cm, as expected for stoichiometric TaN. The elemental composition of the films was analyzed using Auger spectroscopy.

Plans for next contract periods include the incorporation of the TaN coating step into a silicon emitter process flow, testing of coated devices and comparison of their performance with that of uncoated emitters. In a parallel way, depositions of thin films of LaB_6, ZrC, TiC and possibly HfC, are planned to be investigated. These films can be obtained in-house by e-beam evaporation. Suppliers of the materials in the form suitable for use as sources in e-beam evaporation processes have been identified.

4.3 Using some of the results from the process integration analysis, a new round of numerical simulations of the electric fields in the emitter array structures was performed. These incorporated the statistical variation of the geometric parameters across large arrays to produce a more realistic prediction of the emission current a given array would produce. When more array emission current data is available, these simulations will be compared with measurements to asses their validity.

IV. Fiscal Status



Expenditures this quarter (4/16/93 - 7/15/93)	$150,732.69
Total expenditures to date (4/16/93 - 7/15/93)	150,732.69
Contract Amount (Option 1)	$454,965.00

Note: Quarterly expenditures based on financial data and contract committments through 6/28/93, and processing costs through 7/15/93.

V. Problem Areas

Achieving yields on large arrays is imperative if the program is to meet the performance criteria set forth by ARPA. Early results are promising, but so far no arrays over 3,255 tips have yielded. Processing experience from the first runs will improve yields in the later runs.

Gate capture of the emission current is an important issue. The fraction of emission current captured by the gate electrode varies, depending on a combination of gate bias, anode bias, anode distance, and the geometry of the tip and gate opening. Whenever a significant current goes through the gate (calculated to be less than 10 uA for each gate opening), the gate metal will melt and the device will fail. Other reasons for gate electron capture may include the tip height and gate opening size of the emitters, spread of the emission area from the tip apex downward as the gate voltage increases, or tip deformation due to joule heating caused by the tip resistance. The problem is still under investigation.

VI. Visits and Technical Presentations

Several closed meetings were held between MCNC staff and its subcontractors. A process design review with MCNC personnel external to the program was held on May 6, 1993. A similar review of the testing process is scheduled for August 8, 1993. Three staff members attended the Vacuum Electronics Review in Washington, DC June 29 – July 1, 1993. One presentation on this project was made outside the direct program participants during the contract time period covered by this report. A staff member presented a poster entitled "Field Emitter Array Process Optimization and Performance Prediction" at the International Vacuum Microelectronics Conference in Newport, Rhode Island July 12 – 15, 1993. The slides from this session are included as Attachment A.

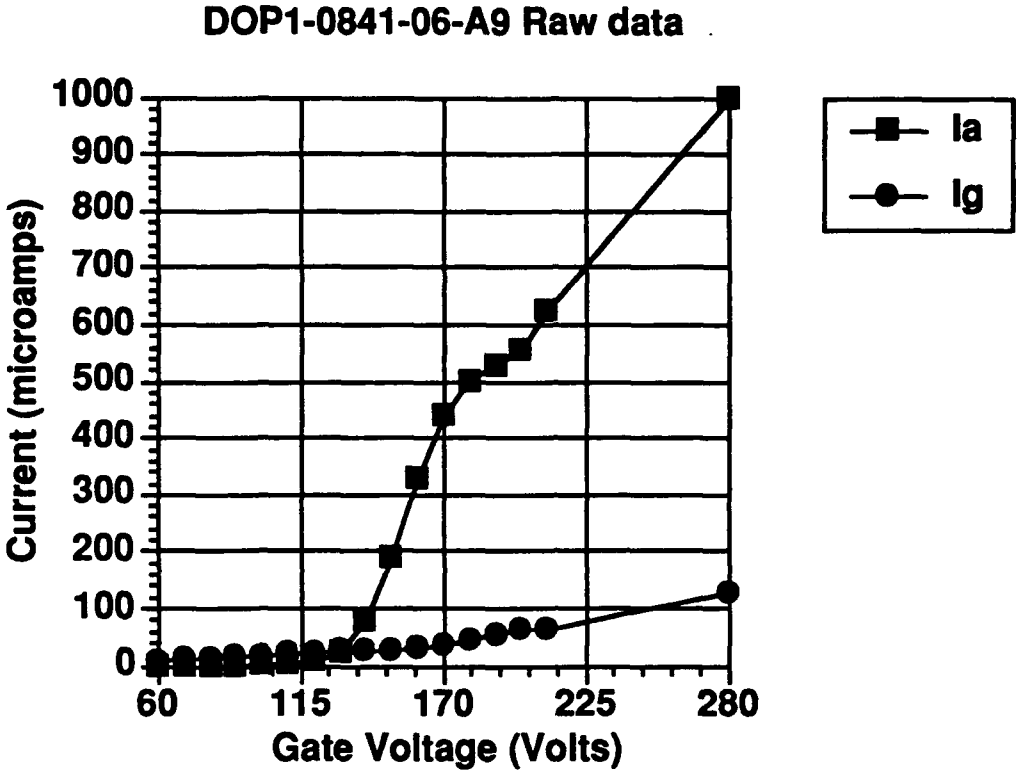


Figure 1: Raw data, 3,255 tip 2 μm column array.

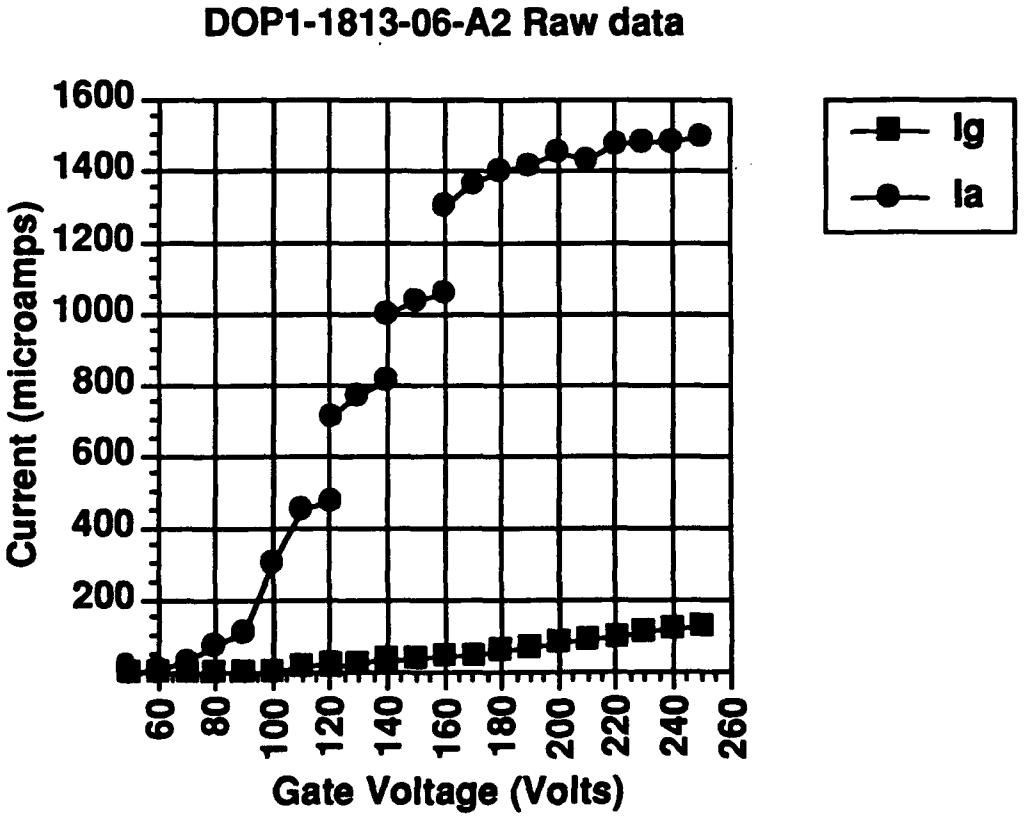


Figure 2: Raw data, 3,255 tip 2 μm column array.

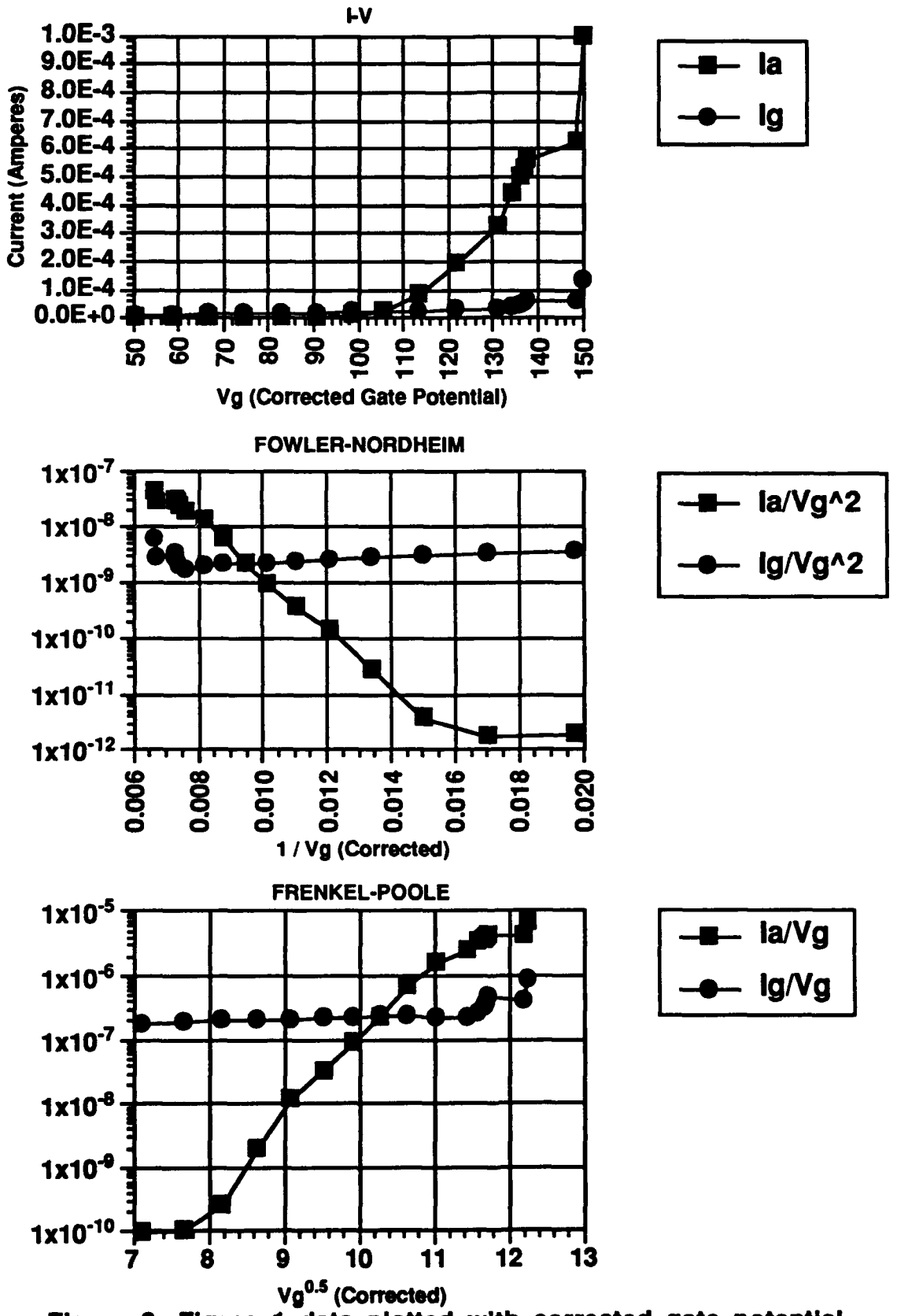


Figure 3: Figure 1 data plotted with corrected gate potential.

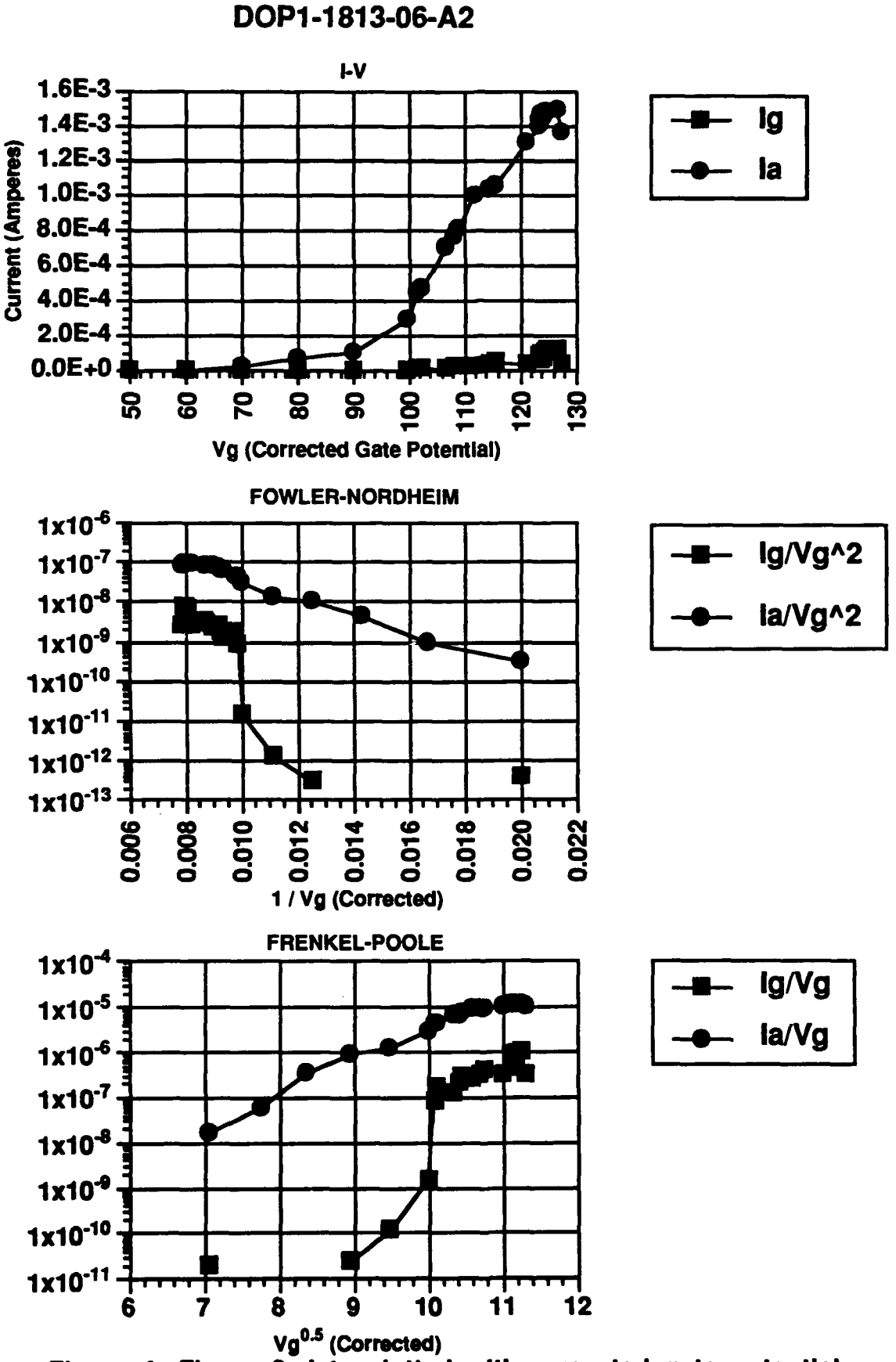


Figure 4: Figure 2 data plotted with corrected gate potential.

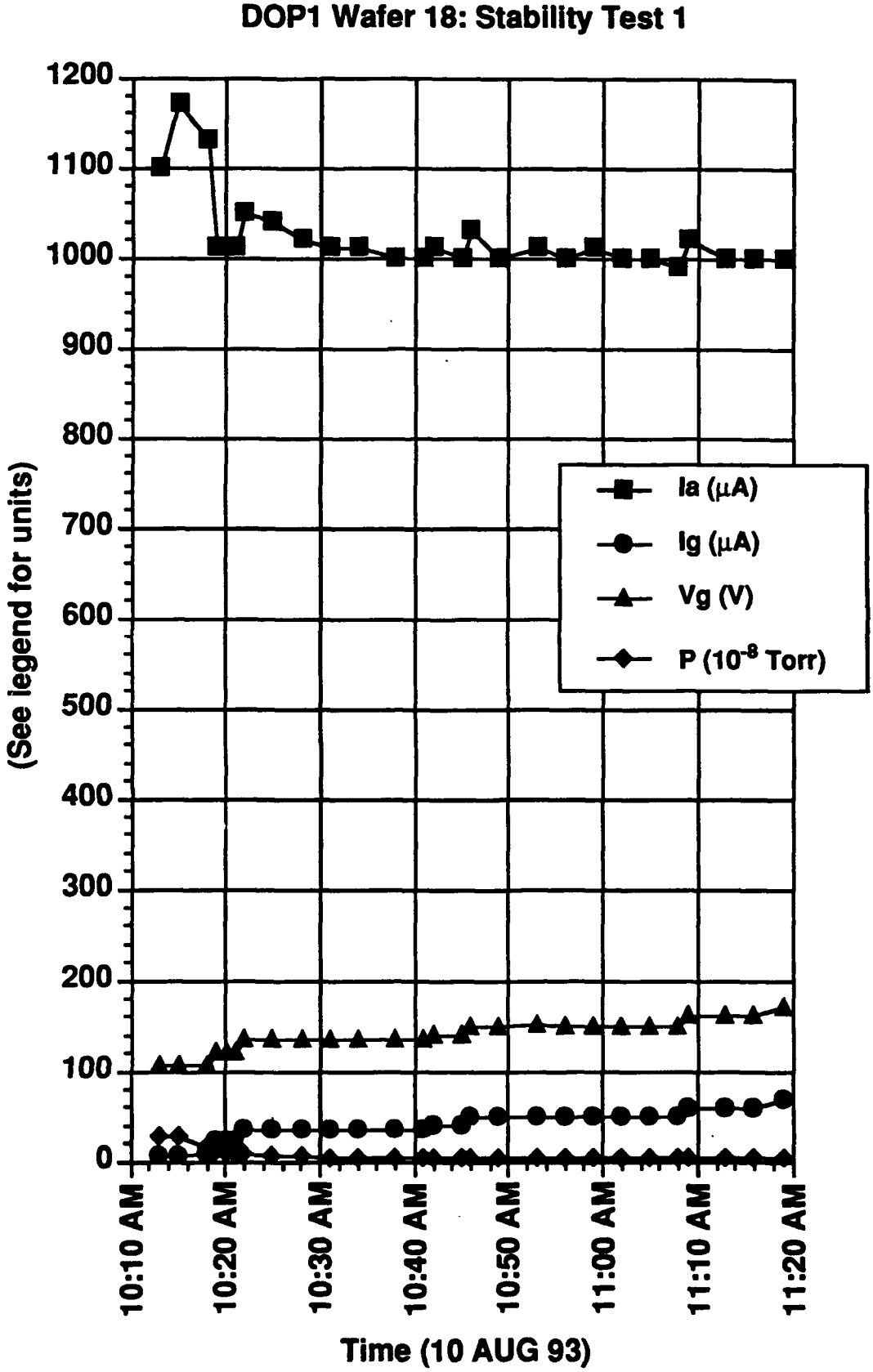


Figure 5: Lifetime test for array in Figures 2 and 4.

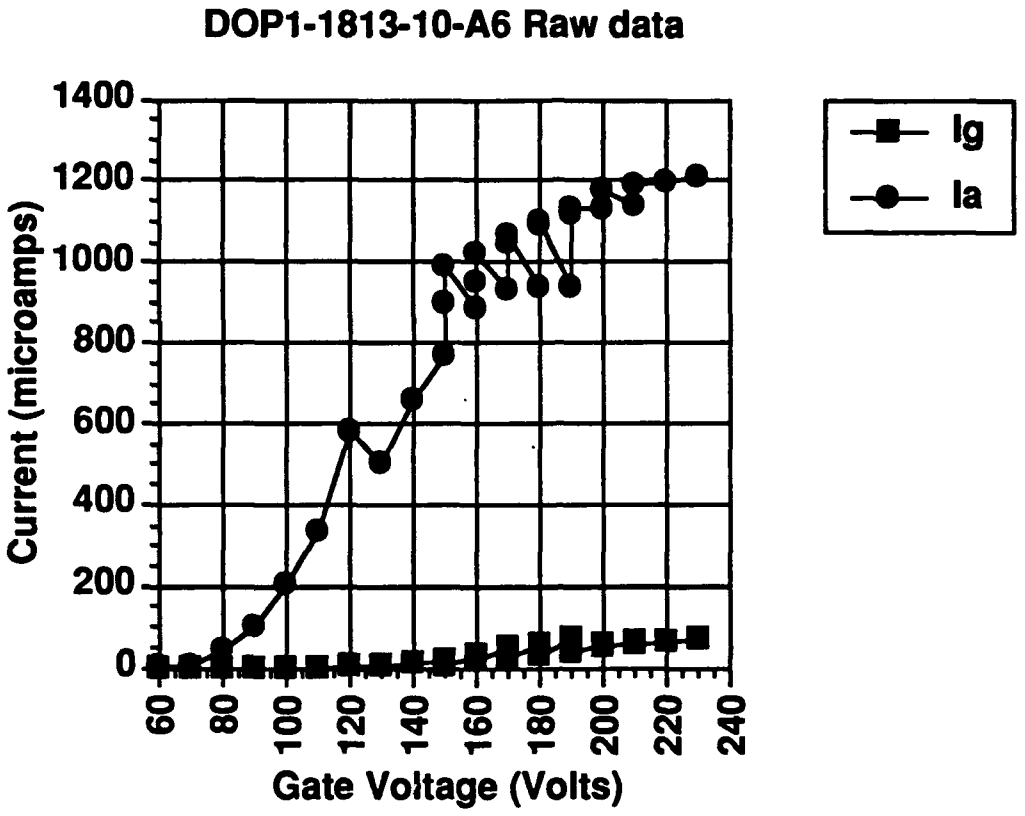


Figure 6: Raw data, 1,197 tip 2 μm column array.

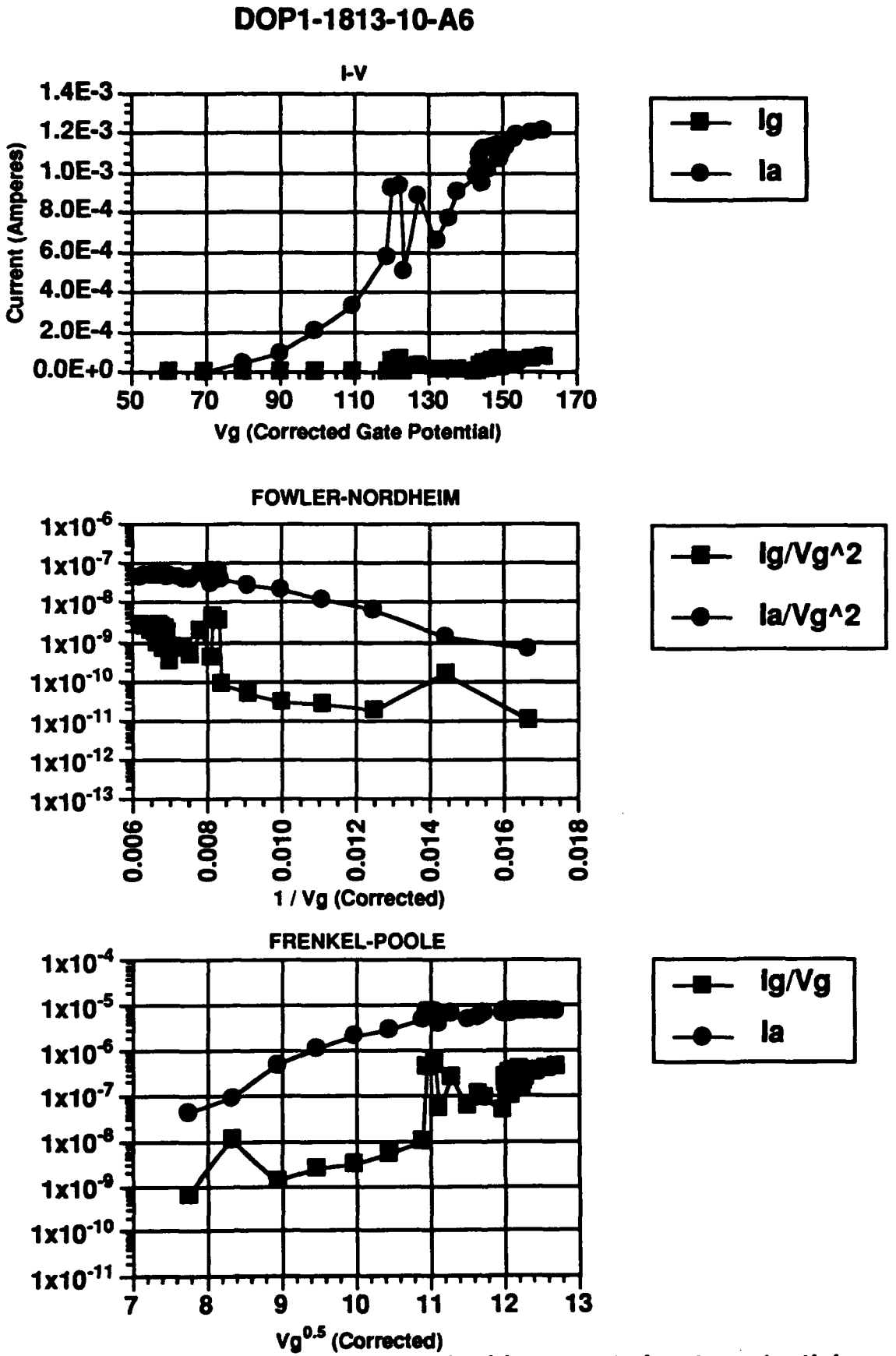


Figure 7: Figure 6 data plotted with corrected gate potential.

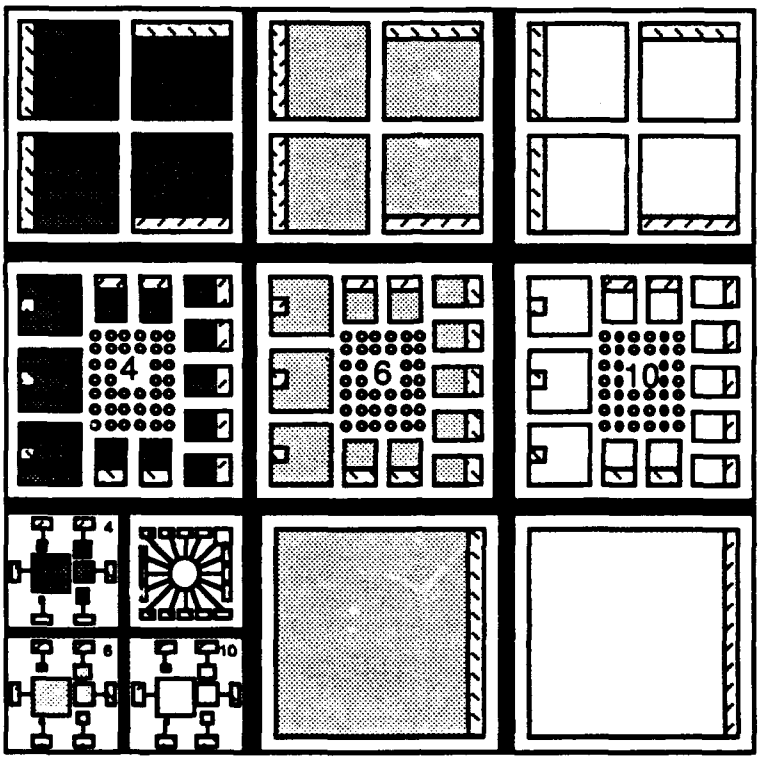


Figure 8. Overall view of the ARPA Option 1 field emitter die design.

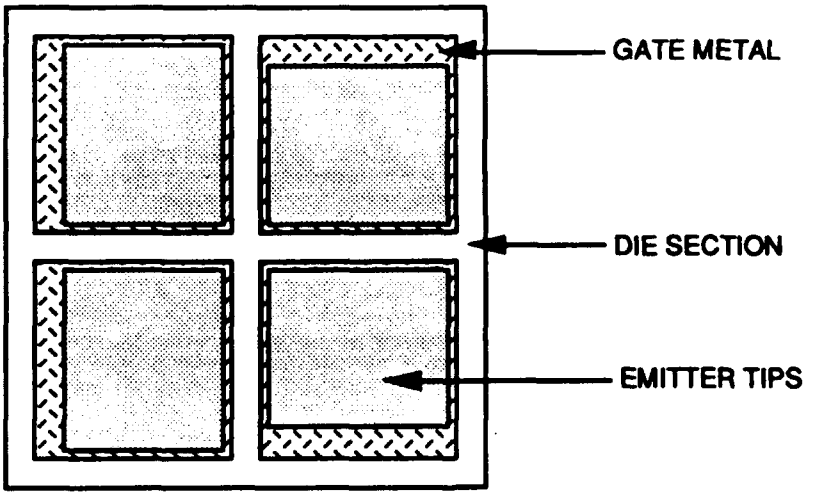


Figure 9. Detail of quad array section.

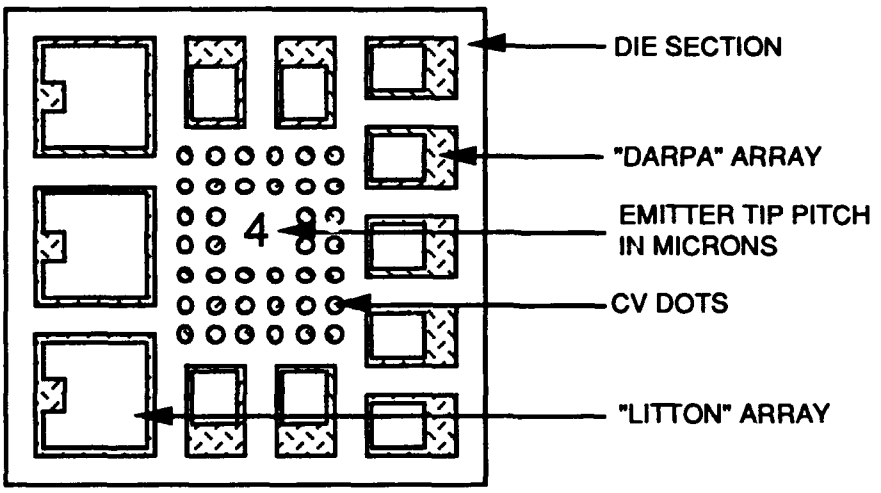


Figure 10. Detail of customer-specific array section.

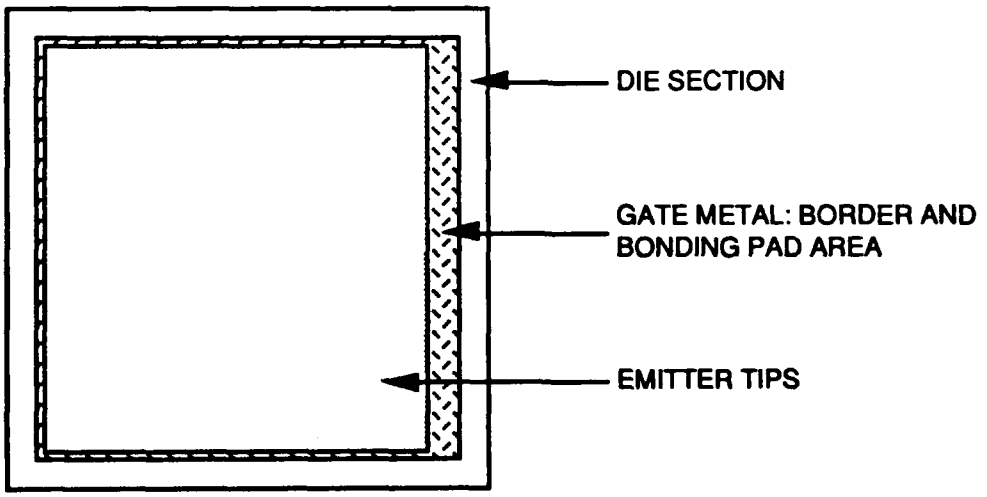


Figure 11. Detail of large array section.

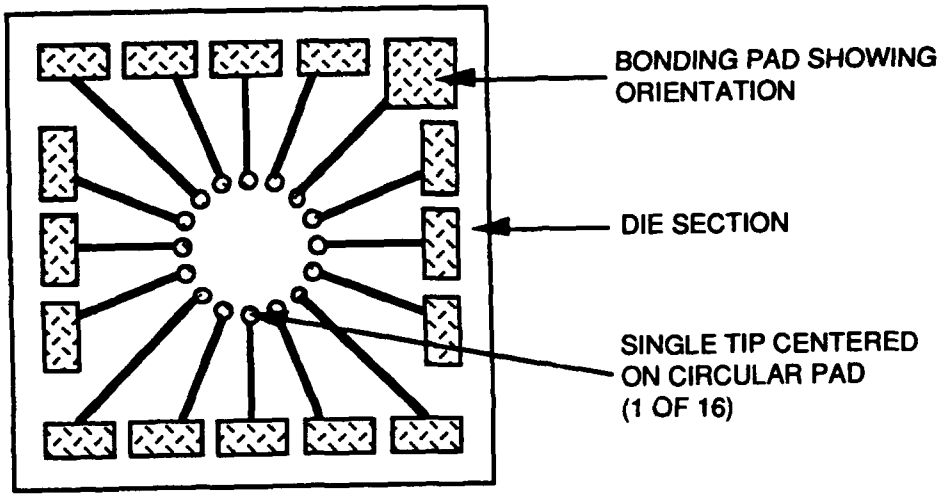


Figure 12. Array for coating studies.

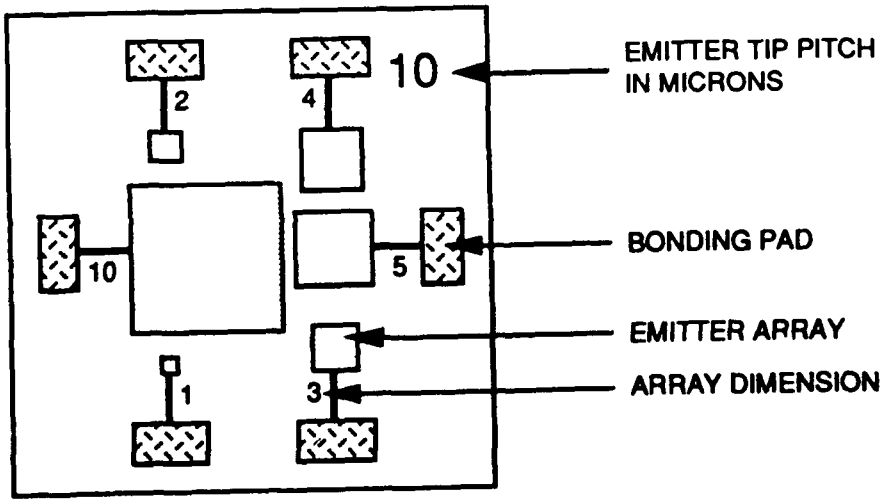


Figure 13. Arrays for per-tip current studies.

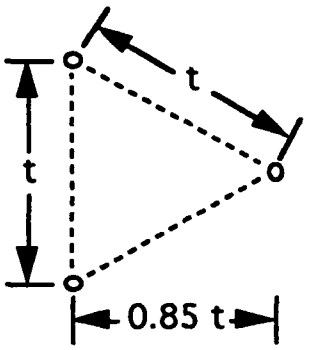


Figure 14. Triangular tip packing.

LIST OF ATTACHMENTS

Attachment A: "Field Emitter Array Process Optimization and Performance Prediction", 14 pages.

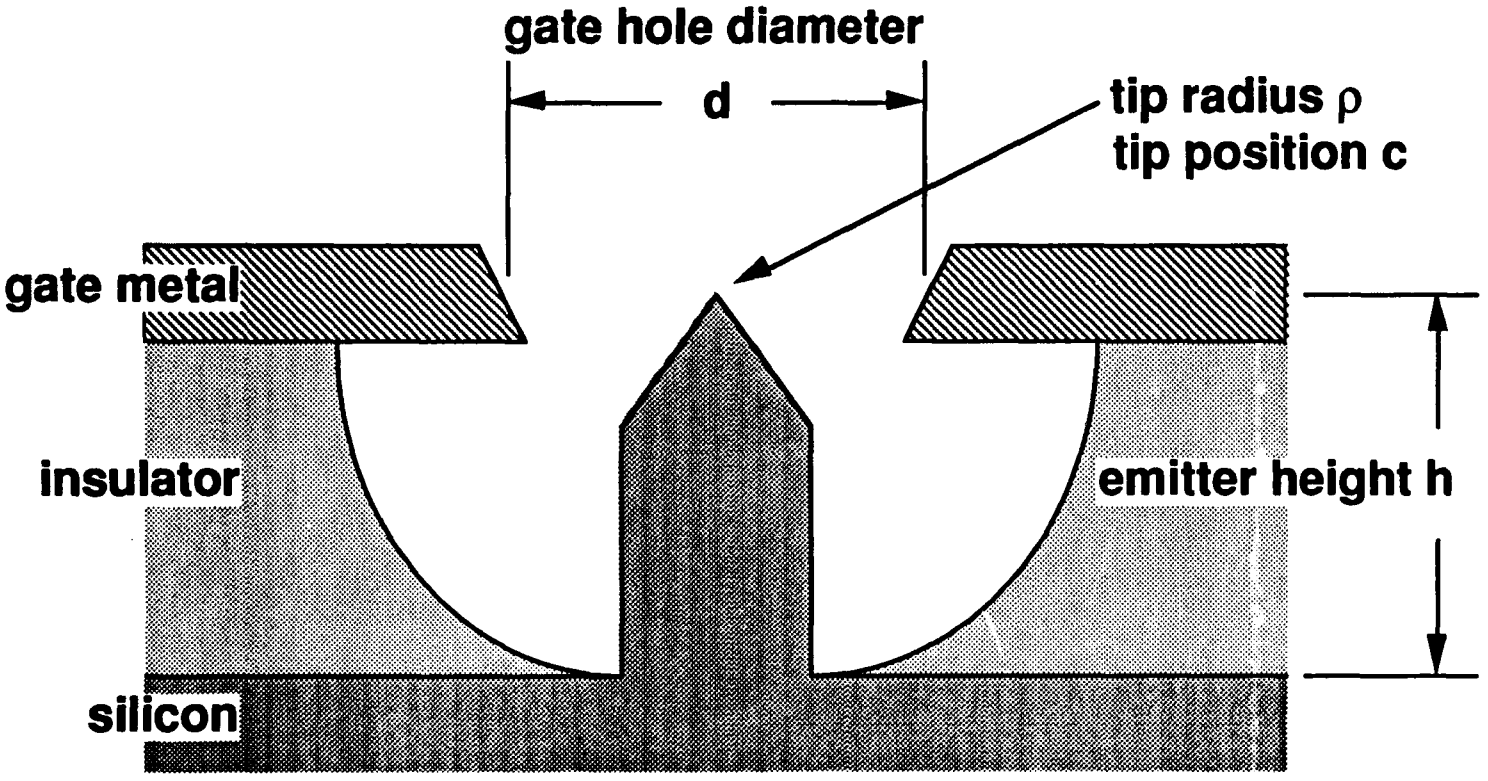
FIELD EMITTER ARRAY PROCESS OPTIMIZATION AND PERFORMANCE PREDICTION

DEV PALMER, CHRIS BALL, DOROTA TEMPLE,
JOE MANCUSI, XUEFENG LIU, AND LINDSEY YADON

SUPPORTED BY ARPA/DSO CONTRACT NUMBER
MDA972-91-C-0028

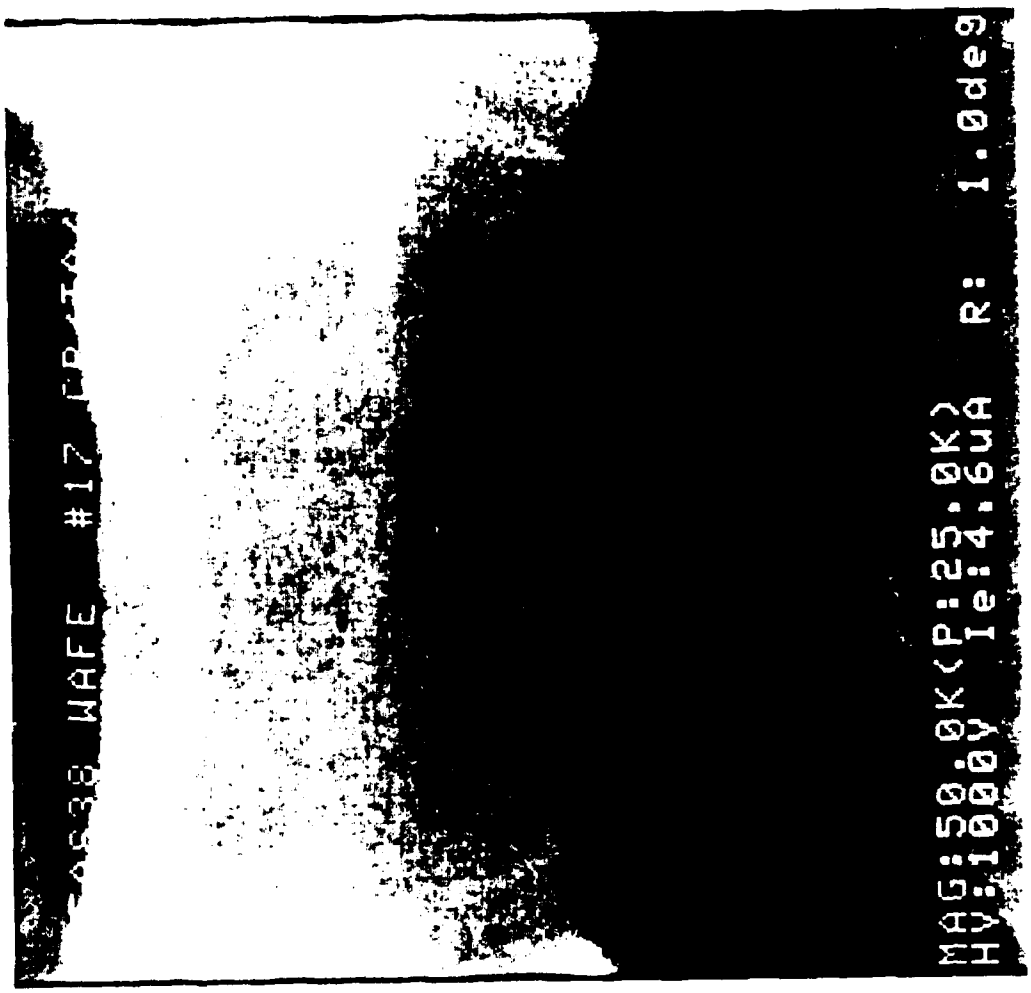
ATTACHMENT A

COLUMN EMITTER GEOMETRY



This figure shows the column emitter geometry of the MCNC silicon field emitter [1, 2]. **c** represents the vertical tip position relative to the center of the thickness of the gate metal. MCNC's self-aligned process produces accurate horizontal centering of the tip. The emitters can be fabricated with a total height **h** up to 10 μm tall using the current process. The tall emitter height is desired to reduce the parallel plate capacitance between the substrate and gate metal, substantially improving high frequency performance.

SEM PHOTO OF FABRICATED COLUMN EMITTER



OBJECTIVES

- UNIFORMLY SHARP TIPS
- YIELD ON LARGE ARRAYS
- TIPS CENTERED VERTICALLY IN GATE METAL
- MINIMUM GATE HOLE DIAMETER

It is well known that the most critical geometric parameter involved in the fabrication and electrical performance of field emitters is the radius of the tip [3, 4, 5]. Even a small variation can have a dramatic effect on the electrical performance of the device [6]. At a given gate voltage, an emitter with a tip diameter half the size of its neighbor's will produce an electric field five times as strong. The primary objectives for our process are uniformly sharp tips and yield on large arrays. Secondary but still advantageous objectives are tips centered vertically in thickness of gate metal, and minimal gate hole diameter. The field emitter program at MCNC uses a statistical analysis of the entire fabrication processflow to optimize their process towards achieving these goals.

STATISTICAL PROCESS CONTROL

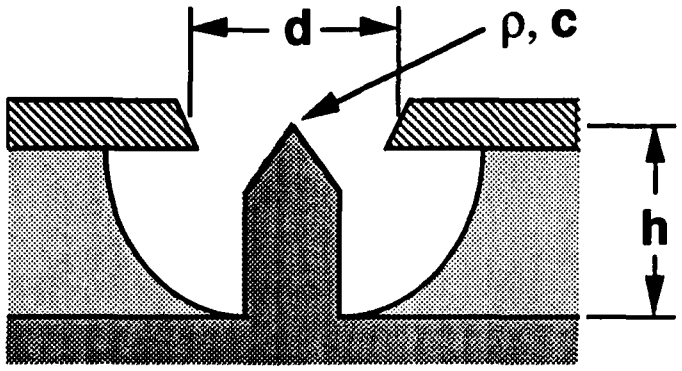
- STATISTICAL ANALYSIS OF EACH STEP IN FABRICATION PROCESS FLOW
- USE KNOWN PROCESS VARIATIONS AND REQUIRED DIMENSIONAL LIMITS TO PICK PROCESSING TARGETS
- PREDICT VARIATIONS IN OTHER PARAMETERS

$$T = \mathbf{MSOW} + \sqrt{\Delta V_1^2 + \Delta V_2^2 + \cdots}$$

MIN - MAX

Statistical process control (SPC) is an engineering technique in which known process variations and required dimensional limits are used to pick processing targets at each step so that the dimensions of the final structure can be reasonably estimated. At MCNC, quite a large number of silicon field emitters have been fabricated, and statistics on the variations in each process have been compiled. By examining the individual process variations, a statistical distribution of the resulting geometries can be predicted. With the results from this type of analysis, electrical characteristics can be predicted using numerical methods such as finite element analysis to calculate the electric fields in a given structure. Ultimately, a matrix of values can be generated which gives a realistic distribution of electrical characteristics resulting from processing variations.

A PRIORI PROCESSING PREDICTIONS



ρ = 100 Å

d: μ = 2.86 μm, σ = 0.095 μm

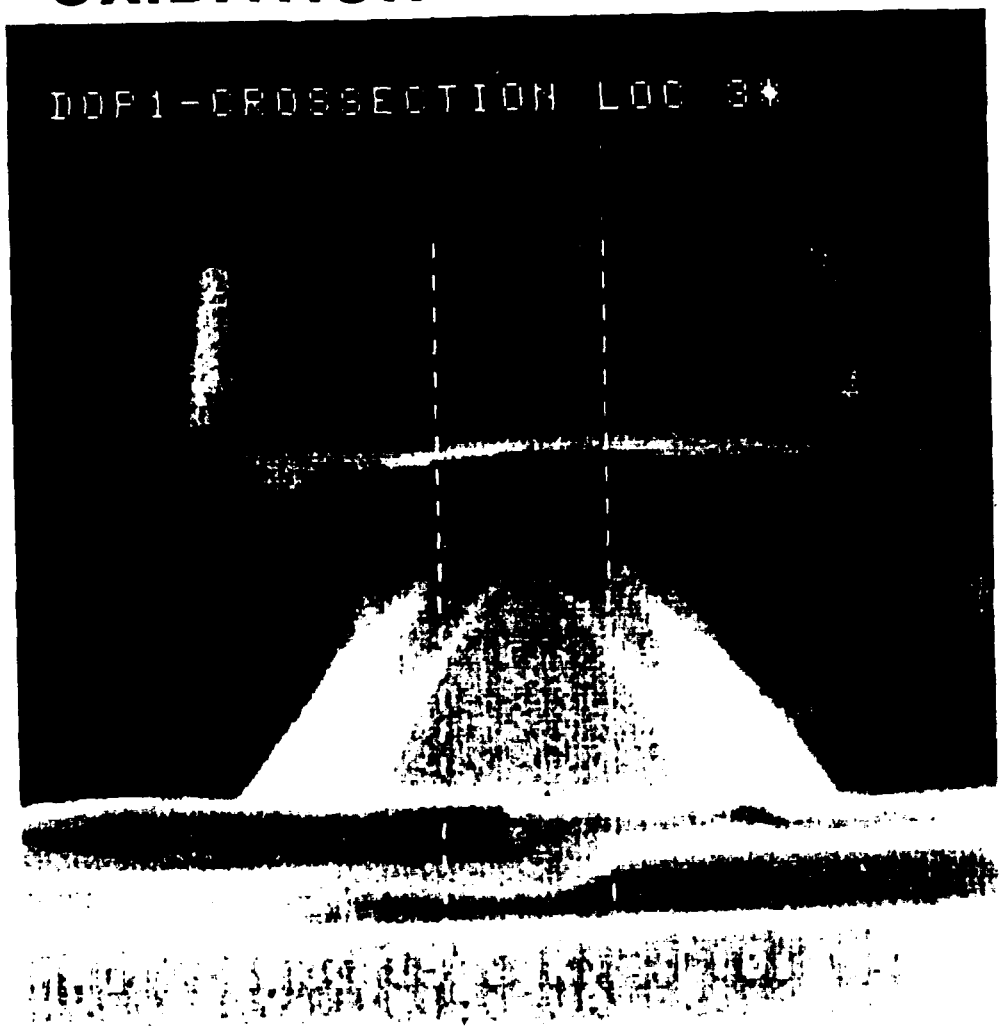
h: μ = 2.00 μm, σ = 0.225 μm

c: μ = 0.00 μm, σ = 0.262 μm

Using SPC, we have designed a process that should give us a field emitter with the distributions of geometric parameters shown here. The process is designed to produce tips of less than 100 Å tip radius.

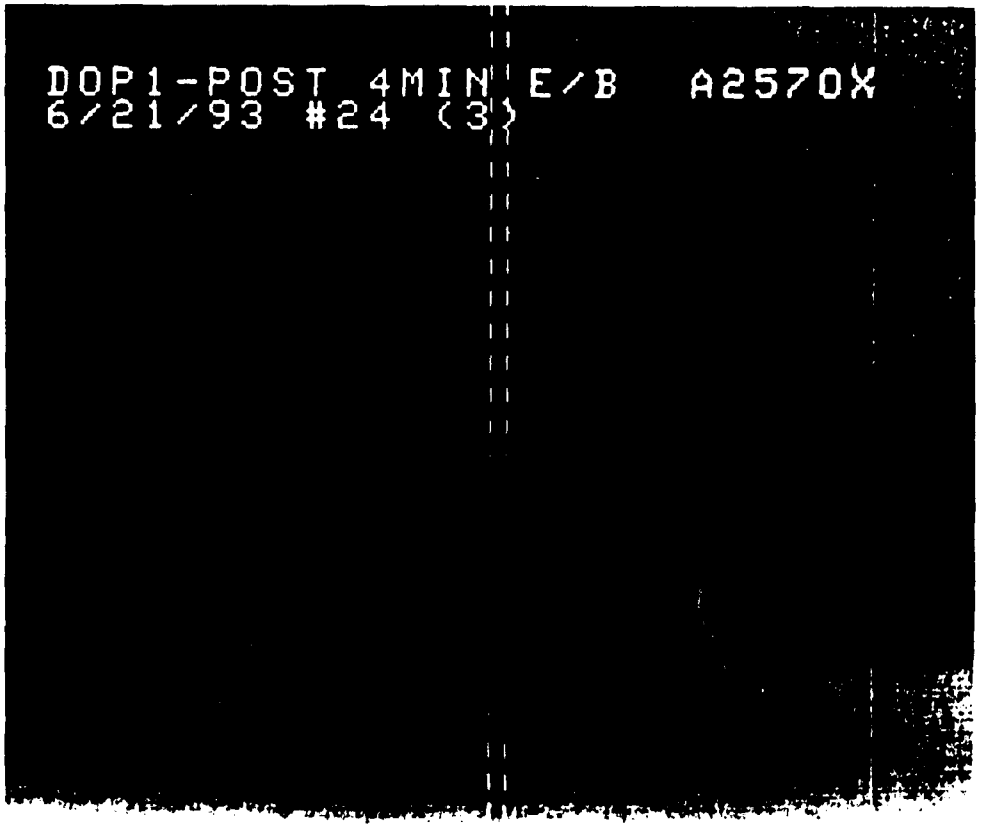
ATTACHMENT A

TIP UNIFORMITY BEFORE OXIDATION SHARPENING



μ = 2600 Å, σ = 280 Å

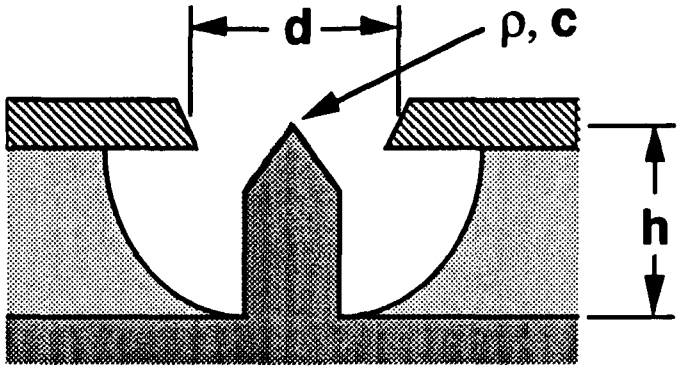
TIP UNIFORMITY AFTER FIRST OXIDATION SHARPENING



$\mu = 217$ Å, $\sigma = 55$ Å

ATTACHMENT A

REVISED PROCESSING PREDICTIONS



ρ = 200 Å

d: μ = 2.93 μm, σ = 0.078 μm

h: μ = 2.00 μm, σ = 0.104 μm

c: μ = 0.00 μm, σ = 0.135 μm

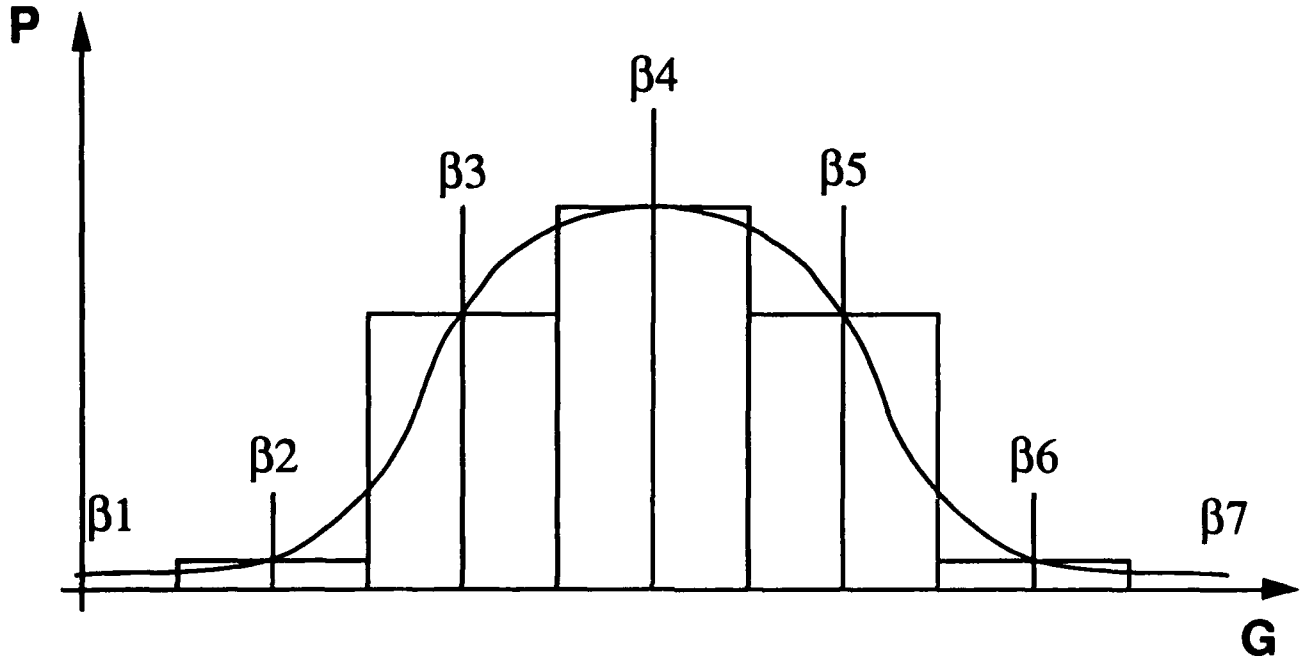
Using measured statistics on a current run rather than the *a priori* data, predictions of the geometric parameters were revised as shown here. The dominating factor in determining these geometries is the initial photolithography. Better uniformity than our earlier statistics would have indicated was achieved partially because of improvements in the available lithographic tools.

PROJECTED YIELD AT 4.6 σ CONTROL

TIPS IN ARRAY	YIELD (%)
100	99.96
1,197	99.50
6,648	97.20
83,850	65.00
232,630	2.00

With 4.6 sigma control on the processflow, projected yields for some of the arrays are shown in the table above. Arrays below 100 tips should achieve virtually 100% yield. For the largest arrays in the mask, only a 2% yield is projected. However, this should be sufficient to provide working devices for testing.

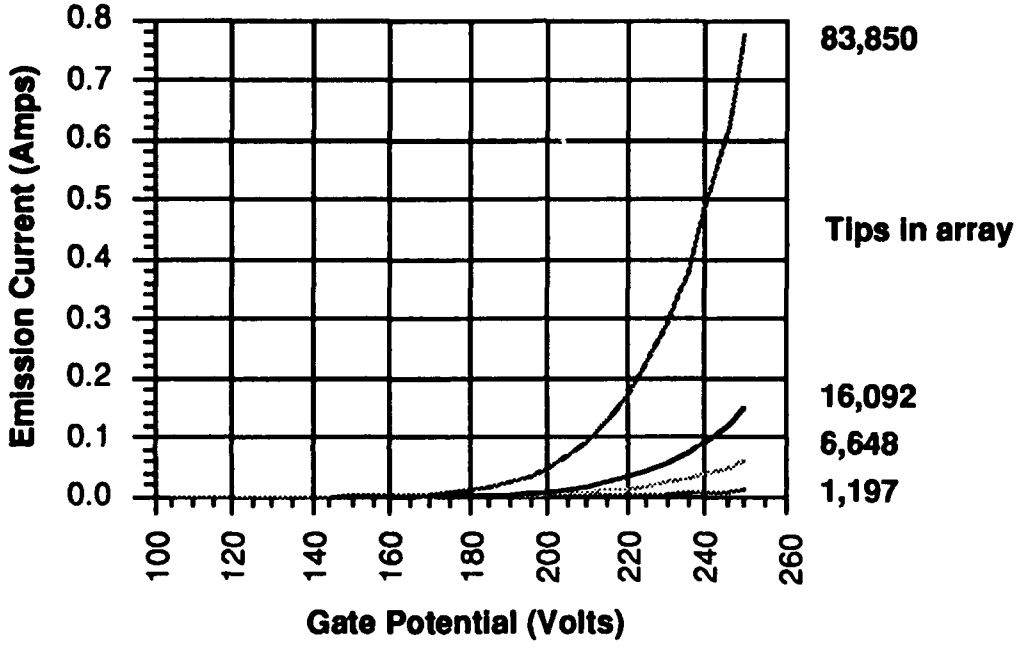
RANGE OF β OVER 3 σ GEOMETRIC VARIATION



$$J_T = N\left[\, J(\beta 1,\, V)\, P(\beta 1) + J(\beta 2,\, V)\, P(\beta 2) + \cdots\right]$$

A typical probability distribution curve is shown above. The x-axis, labeled **G**, represents variations in the geometric parameters of the devices, while the y-axis, labeled **P**, represents the probability of occurrence of a particular geometry. At several points, the field enhancement factor ß is calculated. A statistical version of the Fowler-Nordheim equation for the total array current density J_T can be written as shown. This equation is a linear combination of F-N equations, each a function of a particular ß and voltage, multiplied by the probability of occurrence of that ß. The sum is then multiplied by the number of tips in the array, giving the total F-N current density for the array taking into account the statistical variation between the individual tips. This can be converted to a total current by multiplying by the emission area of the tip, often taken to be a disk with radius ρ [7].

PREDICTED I-V CURVES



Predicted total emission current is shown in this graph. Total number of tips in the arrays range from about 1,200 to almost 84,000. The smallest array will deliver current in the 5–10 mA range, and the largest may supply nearly 0.75 A at a gate potential of 250 V or less.

STATISTICAL PROCESS CONTROL GIVES

- PREDICTABLY SHARP TIPS
- IMPROVED YIELD ON LARGE ARRAYS
- STATISTICAL DISTRIBUTION OF GEOMETRIC PARAMETERS
- STATISTICAL PREDICTION OF ARRAY CURRENT

This research is supported by ARPA/DSO Contract Number MDA972-91-C-0028 under the supervision of Dr. Bertram Hui at ARPA/DSO and Dr. Robert Parker at the NRL. Joe Mancusi is with the Electrical Engineering Department at Duke University. The remaining authors are with the MCNC Center for Microelectronic Systems Technologies. The authors would like to thank Mark Kellam, Frank Lee, Gary McGuire, and Dave Vellenga at MCNC/CMST for their valuable contributions to this work.

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ATTACHMENT A